IN THE CLAIMS:

The text of all pending claims, (including withdrawn claims) is set forth below. Cancelled and not entered claims are indicated with claim number and status only. The claims as listed below show added text with underlining and deleted text with ~~strikethrough~~. The status of each claim is indicated with one of (original), (currently amended), (cancelled), (withdrawn), (new), (previously presented), or (not entered).

1. (Previously Presented) A microcomputer comprising:

a nonvolatile memory including at least a first storage area and a second storage area in which delete and write of data is electrically performed independently, wherein

a plurality of interrupt vectors indicating respective storage places of a plurality of interrupt programs executed upon requesting of an interrupt is stored in the first storage area, and

a plurality of alternate interrupt vectors corresponding to the respective interrupt vectors is stored in the second storage area;

a central processing unit that has a mechanism to access the nonvolatile memory;

a flag indicating that the first storage area is not accessible; and

a conversion circuit that includes a plurality of registers to which a plurality of addresses indicating respective storage places of the alternate interrupt vectors are set, and that, based on a state of the flag, converts a first address indicating a nonvolatile storage place of the interrupt vector that is accessed by the central processing unit into a second address indicating a nonvolatile storage place of the corresponding alternate interrupt vector by outputting the second address from one of the registers corresponding to the first address.

2. (Cancelled)

3. (Cancelled)

4. (Original) The microcomputer according to claim 1, wherein the conversion circuit comprises hardware that performs a predetermined conversion operation.

5. (Original) The microcomputer according to claim 1, wherein the conversion circuit performs a predetermined conversion operation based on a setting by a software.

6. (Previously Presented) The microcomputer according to claim 1, wherein the nonvolatile memory, the central processing unit, the flag, and the interrupt conversion circuit are integrated on a same semiconductor chip.

7. (Previously Presented) The microcomputer according to claim 1, wherein
the interrupt program is stored in the first storage area,
the interrupt vector indicates a start address of the interrupt program,
the alternate interrupt program that is executed instead of the interrupt program is stored in the second storage area, and
the alternate interrupt vector indicates a start address of the alternate interrupt program.

8. (Previously Presented) The microcomputer according to claim 1, wherein
the interrupt program is stored in the second storage area, and
the interrupt vector and the alternate interrupt vector indicate a start address of the interrupt program.

9. (Original) The microcomputer according to claim 7, wherein a main program is stored in the first storage area.

10. (Original) The microcomputer according to claim 8, wherein a main program is stored in the first storage area.

11. (Original) The microcomputer according to claim 7, wherein a main program is stored in the second storage area.

12. (Original) The microcomputer according to claim 8, wherein a main program is stored in the second storage area.

13. (Original) The microcomputer according to claim 7, wherein a main program is stored in a memory other than the nonvolatile memory.

14. (Original) The microcomputer according to claim 8, wherein a main program is stored in a memory other than the nonvolatile memory.

15. (Previously Presented) A microcomputer comprising:

a nonvolatile memory including at least a first storage area and a second storage area in which delete and write of data is electrically performed independently, wherein

a plurality of interrupt vectors indicating respective storage places of a plurality of interrupt programs executed upon requesting of an interrupt is stored in the first storage area, and

a plurality of alternate interrupt vectors corresponding to the respective interrupt vectors is stored in the second storage area;

a central processing unit that has a mechanism to access the nonvolatile memory;

a flag indicating that the first storage area is not accessible; and

a conversion circuit that includes a first pair of registers for setting a first address range corresponding to the first storage area and a second pair of registers for setting a second address range corresponding to the second storage area, and that, when an address within the first range is accessed by the central processing unit, performs address conversion based on a state of the flag to convert the first address range to the second address range.

16. (Previously Presented) The microcomputer according to claim 15, wherein the conversion circuit performs address conversion individually for a plurality of address ranges, each of the plurality of address ranges including each of the interrupt vectors.

17. (Original) The microcomputer according to claim 15, wherein the conversion circuit comprises hardware that performs a predetermined conversion operation.

18. (Original) The microcomputer according to claim 15, wherein the conversion circuit performs a predetermined conversion operation based on a setting by a software.

19. (Previously Presented) The microcomputer according to claim 15, wherein the nonvolatile memory, the central processing unit, the flag, and the conversion circuit are integrated on a same semiconductor chip.

20. (Previously Presented) The microcomputer according to claim 15, wherein

the interrupt program is stored in the first storage area,

the interrupt vector indicates a start address of the interrupt program,

the alternate interrupt program that is executed instead of the interrupt program is stored in the second storage area, and

the alternate interrupt vector indicates a start address of the alternate interrupt program.

21. (Previously Presented) The microcomputer according to claim 15, wherein

the interrupt program is stored in the second storage area, and

the interrupt vector and the alternate interrupt vector indicate a start address of the interrupt program.

22. (Original) The microcomputer according to claim 20, wherein a main program is stored in the first storage area.

23. (Original) The microcomputer according to claim 21, wherein a main program is stored in the first storage area.

24. (Original) The microcomputer according to claim 20, wherein a main program is stored in the second storage area.

25. (Original) The microcomputer according to claim 21, wherein a main program is stored in the second storage area.

26. (Original) The microcomputer according to claim 20, wherein a main program is stored in a memory other than the nonvolatile memory.

27. (Original) The microcomputer according to claim 21, wherein a main program is stored in a memory other than the nonvolatile memory.

28. (Previously Presented) A microcomputer comprising:

a nonvolatile memory including at least a first storage area and a second storage area in which delete and write of data is electrically performed independently, wherein

a plurality of interrupt vectors indicating respective storage places of a plurality of interrupt programs executed upon requesting of an interrupt is stored in the first storage area, and

a plurality of alternate interrupt vectors corresponding to the respective

interrupt vectors is stored in the second storage area;

a central processing unit that has a mechanism to access the nonvolatile memory;

a flag indicating that the first storage area is not accessible; and

a conversion circuit that includes a register to which an offset is set, and that converts a first address indicating a nonvolatile storage place of the interrupt vector that is accessed by the central processing unit into a second address indicating a nonvolatile storage place of the corresponding alternate interrupt vector by adding the offset to the first address.

29. (Previously Presented) A microcomputer comprising:

a nonvolatile memory including at least a first storage area and a second storage area in which delete and write of data is electrically performed independently;

a central processing unit that has a mechanism to access the nonvolatile memory;

a flag indicating that the first storage area is not accessible; and

a conversion circuit that, based on a state of the flag, converts an address indicating a nonvolatile storage place of an interrupt vector that is accessed by the central processing unit into an address indicating a nonvolatile storage place of a corresponding alternate interrupt vector.